HYPERION | QUATTRO™ sFPDP

VITA 17.1 and 17.3 Recording Systems

Flexible. High-Speed. **Ready**



Removable Storage

Up to 720TB, NVMe TCG® Opal SSC Encryption-Ready Drives (SEDs)

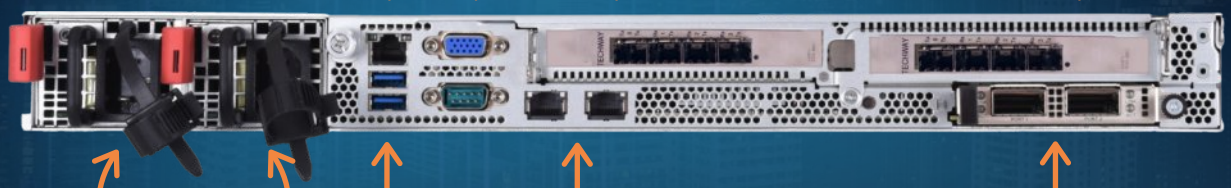
Weight

16.8kg (37.1lbs)

Size (Footprint)

Width	43.9cm (17.3in)
Height	4.3cm (1.7in)
Depth	68cm (26.7in)

Capture & Replay Ports



Power

AC 100-240V/12-6A, 850 Watts
High-Efficiency, 50/60 Hz
Dual Redundant Supply

USB 3.0

1/10 GbE

Optional Rapid Data Offload Interface

daqscribe

Overview

The HYPERION | QUATTRO™ sFPDP system-level and board-level solutions deliver a modular network fabric technology ecosystem for high-performance serial FPDP (sFPDP) data capture, recording, and processing.

The system-level solutions feature VITA 17.1 and VITA 17.3 interface standards and are segmented into two performance tiers:

- HYPERION | QUATTRO-I — VITA 17.1 / 17.3 switchable platforms
- HYPERION | QUATTRO-II — Dedicated high-speed VITA 17.3 platforms

nStudio™ Software Suite

- nRec™ (PN: DSS710P) — Full-rate recording engine.
- nRemote™ — Remote control and management interface
- nPlay™ — Precise packet replay.
- nXplorer™ — Simplified packet handling & Layer-2 monitoring utility.
- nDiscovery™ — Powerful visualization tools & streamlined data management.
- Perpetual runtime software licenses

HYPERION recorders feature one or more QUATTRO™ sFPDP 17.1 or 17.3 board products, enabling lane scalability and performance flexibility.

HYPERION | QUATTRO-I

Switchable. Flexible. Compatible

QUATTRO-I is designed for environments where **interoperability and protocol flexibility** matter as much as performance.

With support for both VITA 17.1 and VITA 17.3, QUATTRO-I enables seamless integration across mixed-generation signal chains without requiring system redesign.

VITA 17.1 / 17.3 Switchable Recorders

Designed to sustain full-rate ingest across all configured lanes within the architectural limits of the Gen2 x4 PCIe subsystem.

Model/Part Number	Description
DDR7950-104-xxT	4 lane (single QUATTRO-I config), VITA 17.1 / 17.3 combo, 1 GB/sec (1U) recorder
DDR7950-108-xxT	8 lane (dual QUATTRO-I config), VITA 17.1 / 17.3 combo, 2 GB/sec (1U) recorder

What's Delivered

- Switchable VITA 17.1 / 17.3 operation
- Up to 6.2 Gb/s per lane
- Deterministic recording up to ~1 GB/s sustained per board
- Proven PCIe Gen2 architecture
- Flexible integration without sacrificing compatibility

Best Fit For

- Legacy radar and telemetry systems
- Mixed VITA 17.1 / 17.3 deployments
- Lab integration and system validation
- Incremental modernization programs
- Controlled-throughput applications

HYPERION | QUATTRO-II

High-Speed. High-Density. High-Performance.

QUATTRO-II is purpose-built for modern platforms where bandwidth density and sustained recording performance are mission-critical.

Optimized exclusively for high-speed VITA 17.3 operation, QUATTRO-II removes compatibility tradeoffs and focuses on maximum data throughput.

VITA 17.3 High-Speed Recorders

Engineered to sustain full-rate ingest across all configured high-speed lanes, aligned with the PCIe Gen3 x16 and NVMe storage architecture.

Model/Part Number	Description
DDR7950-204-xxT	4 lane (single QUATTRO-II config), VITA 17.3, 10 GB/sec (1U) recorder
DDR7950-208-xxT	8 lane (dual QUATTRO-II config), VITA 17.3, 20 GB/sec (1U) recorder
DDR7960-216-xxT	16 lane (quad QUATTRO-II config), VITA 17.3, 40 GB/sec (2U) recorder

What's Delivered

- Dedicated 10.3125 Gb/s per lane architecture
- ~1224 MB/s effective payload per lane
- 10 GB/s sustained per board
- Scalable to 20 GB/s (1U chassis) and 40 GB/s (2U chassis)
- PCIe Gen3 x16 high-throughput backbone

Best Fit For

- Wideband radar capture
- Electronic warfare (EW)
- High-rate telemetry aggregation
- SIGINT platforms
- Next-generation sensor systems

	HYPERION QUATTRO-I	HYPERION QUATTRO-II
Primary Advantage	Compatibility & Flexibility	Maximum Throughput
Protocol Strategy	Switchable 17.1 / 17.3	Dedicated 17.3 High-Speed
Max Link Rate	6.2 Gb/s	10.3125 Gb/s
Sustained Recording	Up to 20 GB/s (160 Gb/s) aggregate	Up to 40 GB/s (320 Gb/s) aggregate
Ideal Deployment	Mixed / Legacy Systems	Modern High-Bandwidth Platforms
Bus Architecture	PCIe Gen2 x4	PCIe Gen3 x16
Lane Count	4, 8	4, 8, 16

Specification	Description
Mechanical	• 1U chassis - HYPERION | QUATTRO-I/II, 27" depth • 2U chassis - HYPERION | QUATTRO-II, 34" depth • 1U, 2U rail kit included
Environmental	• Operating temperature: 10°C to 35°C • Non-operating temperature: -40°C to 70°C • Humidity: 90% non-condensing at 35°C
Processor & Memory	• AMD EPYC single cpu (1U), dual CPU (2U) • 64GB to 2TB ECC system memory
Timing & Synchronization	• OS time synchronization • Optional SMA interface for PPS • NTP 1/10GbE RJ4S
System Interfaces	• 1/10GbE RJ45 ports, X2 • Dedicated GbE port for IPMI • USB 3.0 (rear), (2) USB 3.0 (front), X2 • VGA 15-pin (up to 1920×1200)
Power	• Slim 1U redundant power supply (1+1) • Input: AC 100–240V, 50/60 Hz • Output: 850W (1U), 2700W (2U) • 80 Plus Platinum efficiency
Regulatory	• FCC (SDoC) Class A • CE Class A • CB / LVD • VCCI • C-Tick
Warranty & Services	• Standard 1-year factory warranty • DS-WTY-1 extended hardware warranty • DS-ASIS Annual Software Maintenance • DS-TRN On-site training (1-day session)
Storage Options	• NVMe TCG® Opal SSC encryption-ready drives (SEDs) • Storage capacity 8TB to 720TB • Additional storage drive pack option available
Data Offload Options	• Optional dual QSFP28 Ethernet data offload (OCP 3.0) /N1 option

QUATTRO™ sFPDP PCIe Interface Boards

Board Architecture Segmentation

Feature	QUATTRO-I (DRV104)	QUATTRO-II (DRV204)
Protocol	VITA 17.1 / 17.3 (switchable)	VITA 17.3
FPGA Architecture	Kintex-7	Kintex Ultrascale+
PCIe Interface	Gen2 x4	Gen3 x16
Max Link Speed	6.2 Gb/s	10.3125 Gb/s
Data Throughput	1 GB/s	10 GB/s
Intended Board Use	Mixed / Legacy Systems	Modern (High-Speed) Programs

QUATTRO-II platforms are optimized for high-speed VITA 17.3 operation to maximize throughput and simplify FPGA resource allocation.

QUATTRO-I VITA 17.1 / 17.3 Combo Board

- 4 × sFPDP lanes
- Up to 6.2 Gb/s per lane
- VITA 17.1 / 17.3 switchable
- PCIe Gen2 x4 interface
- Up to ~1 GB/sec
- sustained host throughput
- Linux drivers and SDK included



DRV104 | 4 lane, VITA 17.1 / 17.3 combo, 1 GB/sec board

Throughput is bounded by the PCIe Gen2 x4 interface and may be further limited by host system architecture.

Speed Link Profile QUATTRO-I VITA 17.1 Board Config

Active Lanes	Link Rate per Lane (Gb/s)	Payload Bandwidth per Lane (MB/s)	Aggregate Payload (MB/s)
4	1.0 – 2.5	~100 – 250	~400 – 1000
3	1.0 – 3.125	~100 – 312.5	~300 – 937.5
2	1.0 – 5.0	~100 – 500	~200 – 1000
1	1.0 – 6.2	~100 – 620	~100 – 620

Speed Link Profile: QUATTRO-I VITA 17.3 Board Config

Active Lanes	Link Rate per Lane (Gb/s)	Payload Bandwidth per Lane (MB/s)	Aggregate Payload (MB/s)
4	1.0 – 2.5	~118 – 296	~472 – 1184
3	1.0 – 3.125	~118 – 371	~354 – 1113
2	1.0 – 5.0	~118 – 593	~236 – 1186
1	1.0 – 6.2	~118 – 736	~118 – 736

Note: Sustained host ingest is limited to **~1.0 GB/s** due to PCIe Gen2 x4 architecture.

QUATTRO-II VITA 17.3 High-Speed Board

- 4 × sFPDP lanes
- 10.3125 Gb/s per lane
- Dedicated VITA 17.3 implementation
- PCIe Gen3 x16 interface
- Sustained 10 GB/sec host throughput
- Linux drivers and SDK included



DRV204 | 4 lane, VITA 17.3 high-speed, 10 GB/sec board

Throughput is bounded by the PCIe Gen3 x16 interface and may be further limited by host system architecture.

Speed Link Profile: QUATTRO-II VITA 17.3 Board

Active Lanes	Link Rate per Lane (Gb/s)	Payload Bandwidth per Lane (MB/s)	Aggregate Payload (MB/s)
4	10.3125	~1224	~1224
3	10.3125	~1224	~2448
2	10.3125	~1224	~3672
1	10.3125	~1224	~4896

Sustained Host Ingest (4-lane board)**: ~10 GB/s**
(Limited by PCIe Gen3 x16 and storage subsystem architecture)

Note: The payload bandwidth values shown are effective payload throughput after protocol framing and control overhead, and may therefore be lower than the theoretical payload derived solely from line rate and encoding efficiency. Values are provided for sizing and planning; sustained recorder ingest is additionally bounded by PCIe and storage subsystem architecture.

(Reference: ~1224 MB/s per lane corresponds to ~9.79 Gb/s effective payload, or ~94.96% of 10.3125 Gb/s line rate.)